UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

| APPLICATION NO.  | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|------------------|
| 10/810,035   | 03/26/2004  | Albert S. Weiner     | 2800.450US1         | 8458             |
| 76287 7590 10/16/2008<br>SCHWEGMAN, LUNDBERG & WOESSNER / ATMEL<br>P.O. BOX 2938 |             |                      | EXAMINER            |                  |
|  |             |                      | NGUYEN, THINH T     |                  |
| MINNEAPOLIS, MN 55402  |             |                      | ART UNIT            | PAPER NUMBER     |
|  |             |                      | 2818                |                  |
|  |             |                      |                     |                  |
|  |             |                      | MAIL DATE           | DELIVERY MODE    |
|  |             |                      | 10/16/2008          | PAPER            |

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

|  | Application No.   | Applicant(s)   |  |  |  |
|--|---|--|--|--|--|
|  | 10/810,035  | WEINER, ALBERT S.  |  |  |  |
| Office Action Summary  | Examiner  | Art Unit   |  |  |  |
|  | THINH T. NGUYEN   | 2818   |  |  |  |
| The MAILING DATE of this communication app<br>Period for Reply   | ears on the cover sheet with the c  | orrespondence address  |  |  |  |
| A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA  - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period w  - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).   | ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be time will apply and will expire SIX (6) MONTHS from cause the application to become ABANDONEI | l. lely filed the mailing date of this communication. (35 U.S.C. § 133). |  |  |  |
| Status   |   |  |  |  |  |
| Responsive to communication(s) filed on 29 Second 2a) This action is <b>FINAL</b> . 2b) ▼ This 3) Since this application is in condition for allowant closed in accordance with the practice under Expression 1.   | action is non-final.<br>nce except for formal matters, pro  |  |  |  |  |
| Disposition of Claims  |   |  |  |  |  |
| 4) ☐ Claim(s) 1,3-10 and 20-31 is/are pending in the 4a) Of the above claim(s) 20-30 is/are withdraw 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1,3-10 and 20-30 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or   | n from consideration.   |  |  |  |  |
| · · · <u> </u>   | •   |  |  |  |  |
| 9) The specification is objected to by the Examiner 10) The drawing(s) filed on is/are: a) access Applicant may not request that any objection to the of Replacement drawing sheet(s) including the correction  11) The oath or declaration is objected to by the Examiner   | epted or b) objected to by the Edrawing(s) be held in abeyance. See on is required if the drawing(s) is obj   | e 37 CFR 1.85(a).<br>ected to. See 37 CFR 1.121(d).                      |  |  |  |
| Priority under 35 U.S.C. § 119   |   |  |  |  |  |
| <ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No.</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul> |   |  |  |  |  |
| Attachment(s)  1) Notice of References Cited (PTO-892)  2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  3) Information Disclosure Statement(s) (PTO/SB/08)  Paper No(s)/Mail Date 6/12/2008.  | 4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:  | te   |  |  |  |

Application/Control Number: 10/810,035 Page 2

Art Unit: 2818

## **DETAILED ACTION**

1. Claims 1,3-10,20-31 are pending in the Application with claims 20-30 withdrawn from consideration as directed to non-elected invention

## Claim Rejections - 35 USC § 103

- 2. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 3. Claims 1,3-4,6,9-10,31 are rejected under 35 U.S.C. §103(a) as being anticipated by Lee et al. (U.S. Patent 6,687,154) thereafter Lee 154 in view of Yang et al. (US patent 6,678,190) thereafter Yang 190

With regard to claim 1, Lee (in fig 7B,fig 7D, in fig 9) discloses all the invention of a transistor memory array comprising:

a first plurality of non-volatile user programmable (fig 7B, transistors 70a and 70b) memory cell including a memory transistor and a select transistor and a second plurality of mask programmed read-only memory cells( fig 7D, transistors 70a and 70b) including a memory

Art Unit: 2818

transistor and a select transistor, the non-volatile memory cells and the read-only memory cells having the same area footprint within a single memory array (column 13 line 13-32).

Missing in Lee 154 is the limitation wherein the second plurality of mask programmed read-only memory cells is formed from a single layer electrode

Yang 190, however, discloses a plurality of mask programmed read-only memory cells that is formed from a single layer electrode (fig 5,fig 3,fig 11,column 1 lines 5-35)

It would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate this feature, as taught by Yang 190, into the Lee 154 device and come up with the invention of claim 5.

The rationale is as the following:

A person skilled in the art at the time the invention was made would have been motivated to take advantages of different features offered by Yang 190( fig 5 to fig 8) column 2 lines 10-40) in order to make the Lee 154 device has more versatility and become a better device.

Noted that Lee discloses a Mask ROM cell and a Flash cell (i.e. user programmable non-volatile cell) using the same process and by shorting the control gate and the floating gate of the Flash cell to make a Mask Rom cell, therefore the two cells inherently have the same footprint and the same area footprint. Noted that transistor 70b in fig 7B and 7D (column 6 line 5) can be used as select transistors.

With regard to claim 3, Lee discloses (in fig 4,column 6 line 5) a memory array wherein the footprint has a longitudinal dimension and a width dimension that are the same for both the first and second pluralities of memory cells. with the select transistor (fig 7B and fig 7D transistor 70b) and memory transistor having a common electrode in each memory cell.

Art Unit: 2818

Noted that in fig 7B and 7D the common electrode is the common Source and Drain ( fig 7B and Fig 7D reference 78 )

With regard to claim 4,Lee discloses (in column 13 lines 1-12)a memory array wherein the read-only memory cells including cells having transistor s with substrates having open channels and cells having substrate with shorted channel.

noted that Rom cell in Lee disclosure can be closed or open using boron implantation ( i.e. either the channel is not implanted by boron or implanted by boron dopant, Lee reference column 6 lines 13-15,column 8 line 51-54 )

With regard to claim 5, as set forth in the rejection of claim 1, Lee discloses a non-volatile memory cell (Lee fig 7B) that has two poly layers meanwhile Yang 190 discloses. That the read only memory cell that has one poly layer. (Yang 190 fig 5-fig 8)

With regard to claim 6, Lee discloses (in fig 6) a memory array of claim wherein the second plurality of read- only memory cells is grouped into rows.

With regard to claim 9,Lee discloses (, fig 7D, column 13 lines 1-12) a memory array wherein the channels in the read-only memory cell are defined by a buried depletion implant in said substrate, the extent of the implant defining open and shorted channels.

With regard to claim 10, Lee discloses (fig 7B, in fig 9,column 6 line 37) a memory array wherein said non-volatile memory transistors are EEPROM transistors.

With regard to claim 7,8 as set forth in the rejection of claim 6, the combined Lee 154 in view of Yang 190 device discloses all the invention of claim 7 and claim 8 except for the condition of programming wherein the group of ROM cells has a first subgroup of Memory cells

Art Unit: 2818

at least one row in first logic state and a second subgroup of memory cells in at least one row second logic state.

It would have been obvious to one of ordinary skill in the art the time the invention was made to set the condition of programming wherein the group of ROM cells has a first subgroup of transistors at least one row in first logic state and a second subgroup of transistors in at least one row second logic state in the Lee 154 in view of Yang 190 device since it has been held that the provision of adjustability when needed, involves only routine skill in the art (Noted that the adjustability skill in this case is a mere routine programming skill of a mask ROM (i.e. set one or set zero) during production to adjust to a particular application, also noted that Lee invention is highly flexible (column 13 lines 48-53) and can be applied to multiple applications(column 1 lines 27-40). Noted that it has been held that the provision of adjustability when needed, required only routine skill in the art. In Re Steven, 101 USPQ 284 (CCPA 1954)

With regard to claim 31,both Lee 154 (the abstract) and Yang 190 (column 1 lines 1-67,column 2 lines 1-10) disclose a plurality of non-volatile user programmable memory cells.

- 4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.
- 5. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

Application/Control Number: 10/810,035 Page 6

Art Unit: 2818

**CONCLUSION** 

6. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The

examiner can normally be reached on 9:30 am - 6:30 pm Monday to Friday. If attempts to reach

the examiner by telephone are unsuccessful, the examiner's supervisor, STEVEN LOKE can be

reached on 571-272-1657. The fax phone numbers for the organization where this application or

proceeding is assigned is 571-273-8300

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval [ PAIR ] system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thinh T Nguyen/ Patent Examiner

Art Unit 2818